CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method comprising: receiving a packet at a network device; pre-fetching a protocol control block (PCB) associated with the packet into a cache of a selected processing unit; queuing the packet for processing; pre-fetching a header associated with the packet into the cache of the selected processing unit; and retrieving the PCB from the cache of the selected processing unit when the selected processing unit is ready to process the packet.

2. (Previously Presented) The method of claim 1, further comprising checking the destination of the interrupt and disabling interrupts from a network interface.

3. (Previously Presented) The method of claim 2, further comprising retrieving the packet header from the cache associated with the selected processing unit when the processing unit is ready to process the packet.

4. (Previously Presented) The method of claim 1, further comprising sending an interrupt to notify the selected processing unit of the receipt of the packet.

5. (Previously Presented) The method of claim 4, wherein the interrupt is a software interrupt.

6. (original) The method of claim 5, further comprising storing the packet in a memory coupled to the processing unit.

7. (original) The method of claim 1, further comprising processing the packet.

8. (Previously Presented) An apparatus comprising: a receive unit to receive a packet; a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet and a header associated with the packet into a cache of a processing unit and queue the packet processing; and the processing unit coupled to the pre-fetch unit to retrieve the PCB and the header from the cache and process the packet.

9. (original) The apparatus of claim 8, wherein the receive unit is a network interface card.

10. (Previously Presented) The apparatus of claim 9, further comprising an interrupt service unit to check the destination of the interrupt, disable further interrupts from the network interface card, initiate a software interrupt, and queue the packet for processing.

11. (canceled).

12. (canceled).

13. (original) The apparatus of claim 8, further comprising an interrupt unit coupled to the receive unit and the processing unit to receive an interrupt from the receive unit and notify the processing unit of the packet.

14. (Currently Amended) An article of manufacture comprising: a machine accessible medium including content that when accessed by a machine causes the machine to: receive a packet; pre-fetch a protocol control block (PCB) associated with the packet and a packet header ~~associated with~~ of the packet into a cache of a processing unit; queue the packet for processing; [[and]] retrieve the PCB from the cache when the processing unit is ready to process the packet; and to pre-fetch a PCB for a packet to be sent when the to-be-sent packet is queued for transmission across a network wherein the PCB for the to-be-sent packet is pre-fetched in response to a send request being initiated for the to-be-sent packet.

15. (Currently Amended) The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to pre-fetch the packet header ~~associated with~~ of the packet into the cache.

16. (original) The article of manufacture of claim 15, wherein the machine-accessible medium further includes content that causes the machine to retrieve the packet header from the cache when the processing unit is ready to process the packet.

17. (original) The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to process the packet.

18. (original) The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to send an interrupt to notify the processing unit of the receipt of the packet.

19. (canceled)

20. (original) The article of manufacture of claim 14, wherein the machine accessible medium further includes content that causes the machine to store the packet in a memory coupled to the processing unit.

21. (Currently amended) A system comprising: a receive unit to receive a packet; a memory coupled to the receive unit to store the received packet; a memory controller coupled to the memory to manage the memory; a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet and a packet header ~~associated with~~ of the packet into a cache of a processor and queue the packet for processing; and a processing unit to retrieve the PCB from the cache of the processor and process the packet and retrieve the packet header when the packet is ready to be processed.

22. (original) The system of claim 21, wherein the receive unit is a network interface card.

23. (canceled)

24. (Currently amended) The system of claim 21, further comprising a send unit to pre-fetch a PCB for a packet to be sent when the to-be-sent packet is queued for transmission across a network ~~wherein the processing unit is to further retrieve the packet header from the cache~~.

25. (original) The system of claim 21, wherein the PCB for the to-be-sent packet is pre-fetched in response to a send request being initiated for the to-be-sent packet ~~further comprising an interrupt unit coupled to the receive unit and the processing unit to receive an interrupt from the receive unit and notify the processing unit of the packet~~.